

# GA-F2A88XN-WIFI

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APU\_VDDIO\_SUS=DDR15V  
APU\_VTT\_SUS=DDRVTT  
APU\_VDDP\_RUN=APU\_VDDR\_RUN=APU\_VDDP  
  
+1.1V\_RUN=FCH\_VDD\_11\_RUN=VCC\_SB  
  
+3.3V\_RUN=VCC3  
+3.3V\_ALW=3VDUAL

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**GIGABYTE™**

Title

**COVER SHEET**

Size

Custm

Document Number

Rev

Date:

Monday, August 19, 2013

Sheet

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of

26

**3.01**

**Model Name:GA-F2A88XN-WIFI**

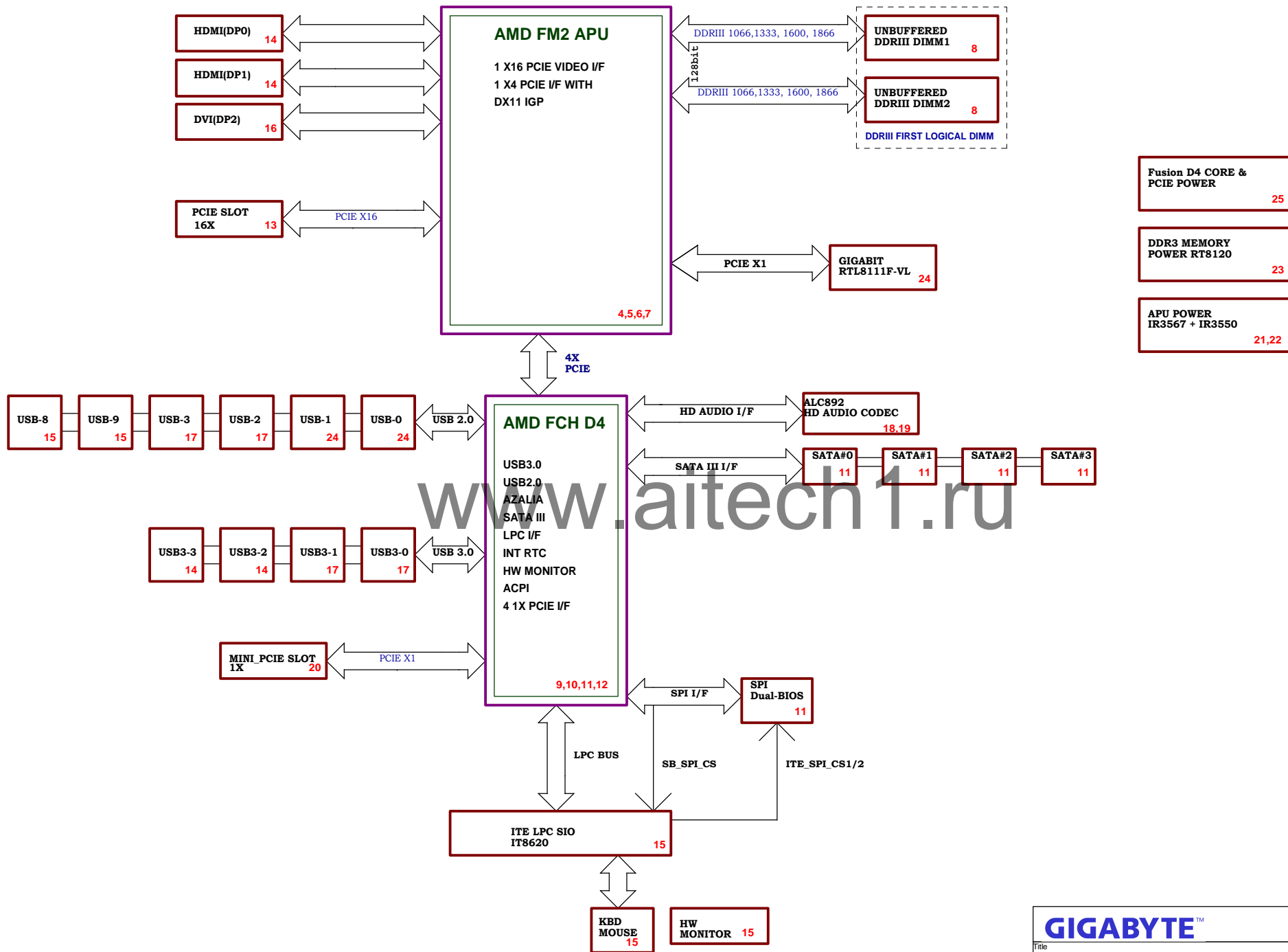
### Component value change history

**Version: 3.01**  
P-Code: U13058-0

[illegible]

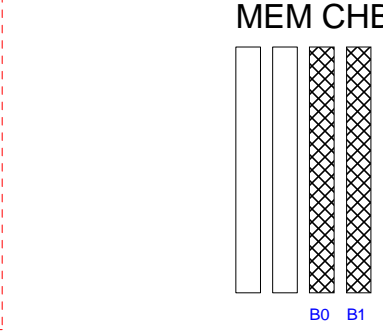
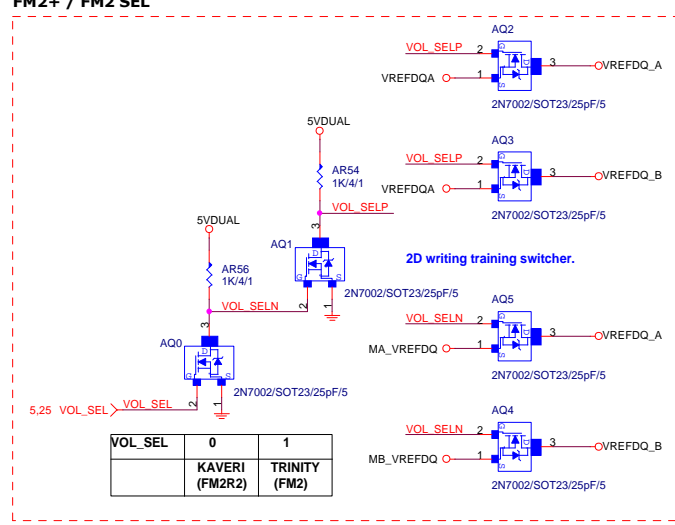
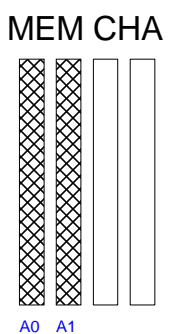
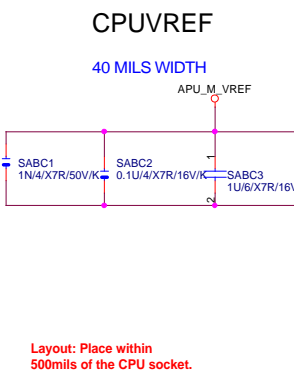
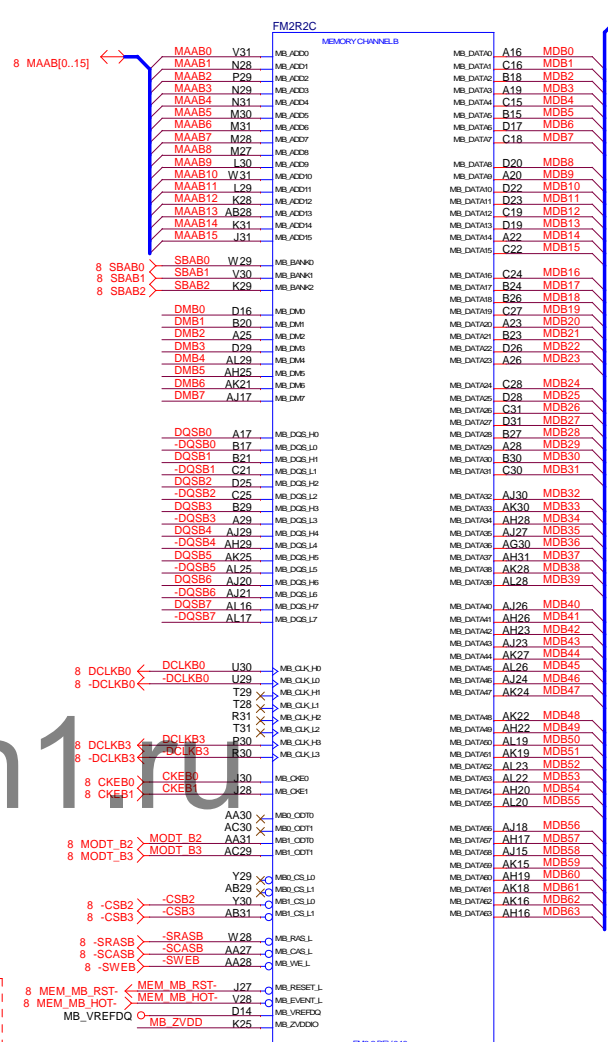
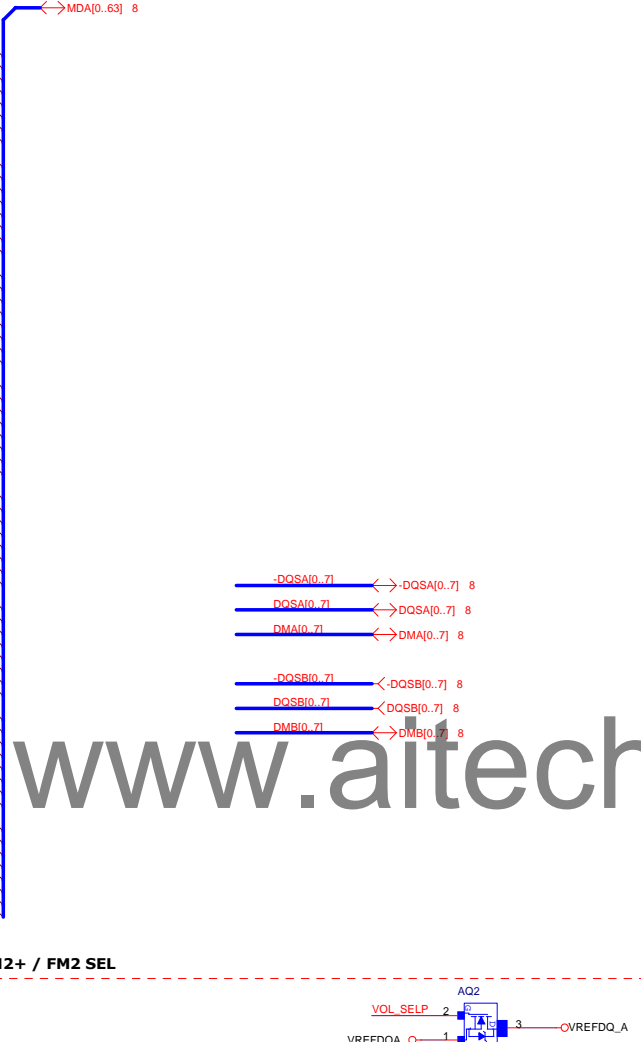
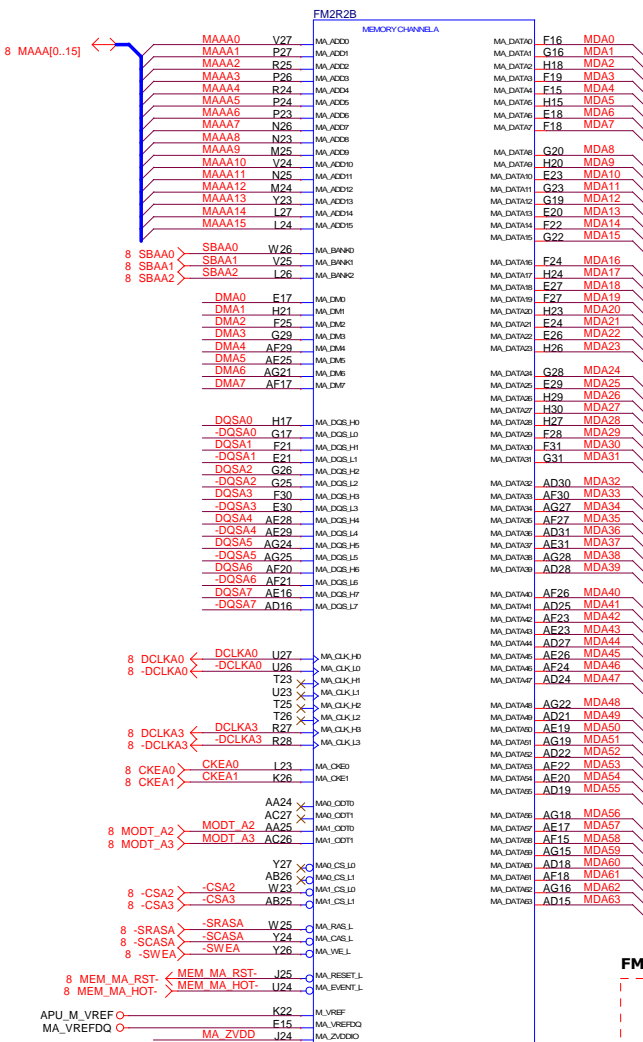
### Circuit or PCB layout change for next version

[illegible]



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Title <b>BLOCK DIAGRAM</b>			
Size Custom	Document Number <b>GA-F2A88XN-WIFI</b>	Rev <b>3.01</b>	
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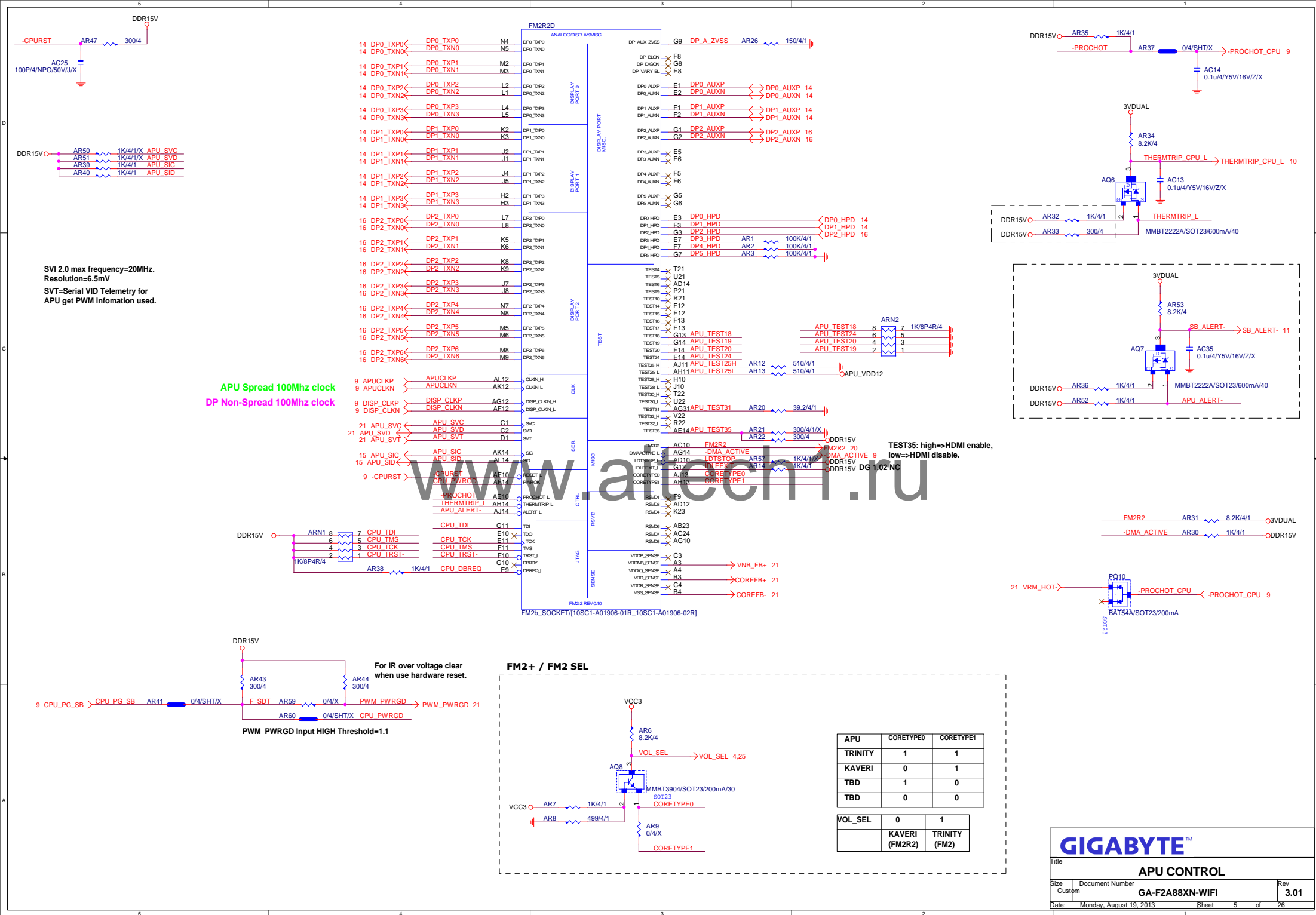


**GIGABYTE™**

Title: **APU DDRIII MEMORY**

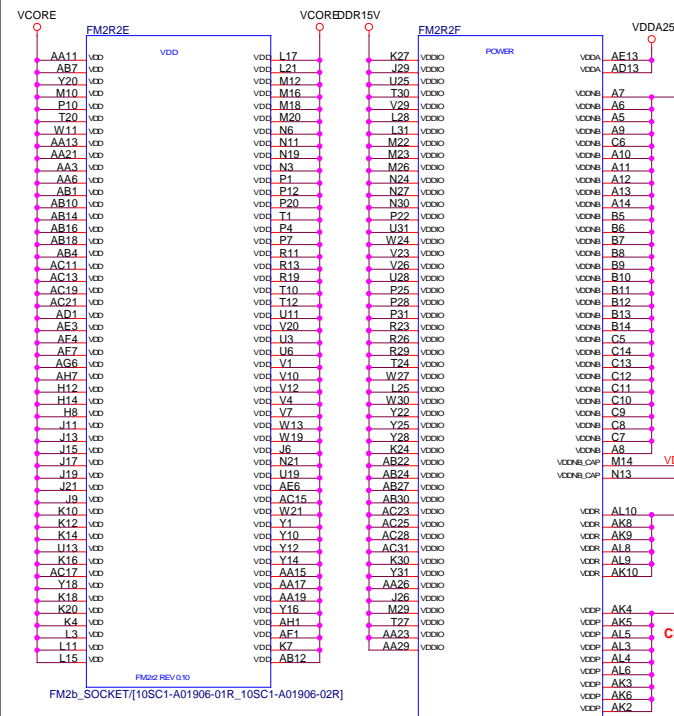
Size: Custom Document Number: **GA-F2A88XN-WIFI** Rev: **3.01**

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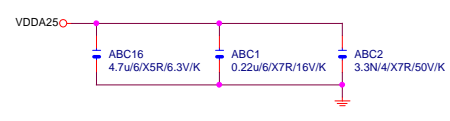




DDR15V=1.25V/1.35V/1.5V(DDR3)

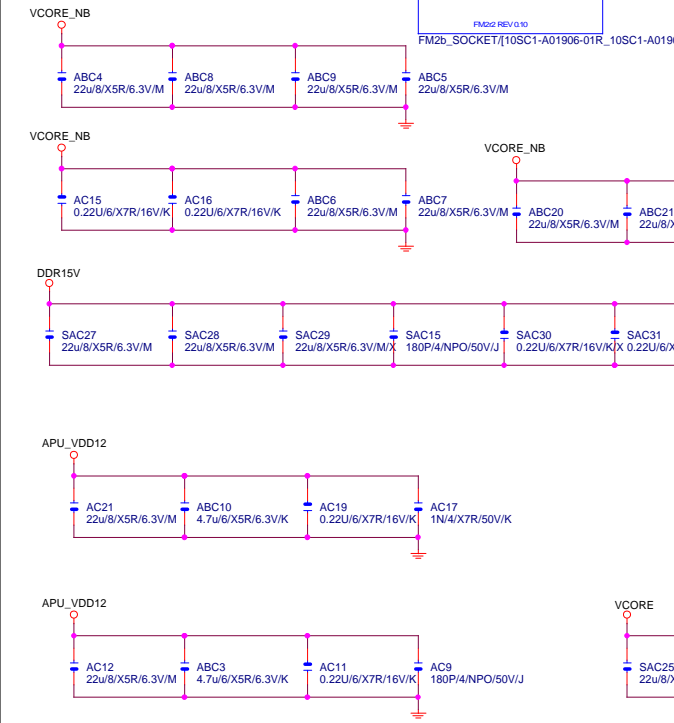
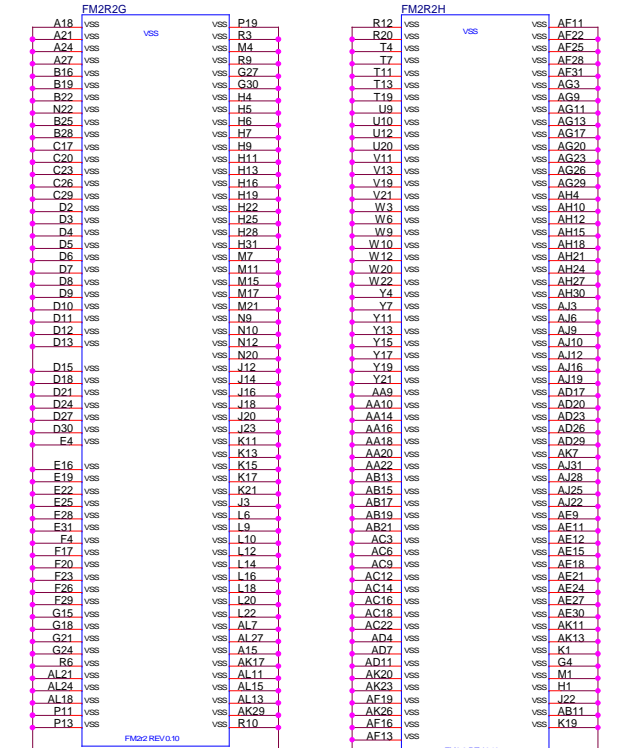


GND:232 pin,  
VCORE:99 pin,  
VCORE\_NB: 30 pin,  
DDR15V:49 pin,  
VDDP:9 pin, VDDR:9  
pin, VDDA25:2 pin,  
VDDNB\_CAP:2  
pin,Total:430 pin.

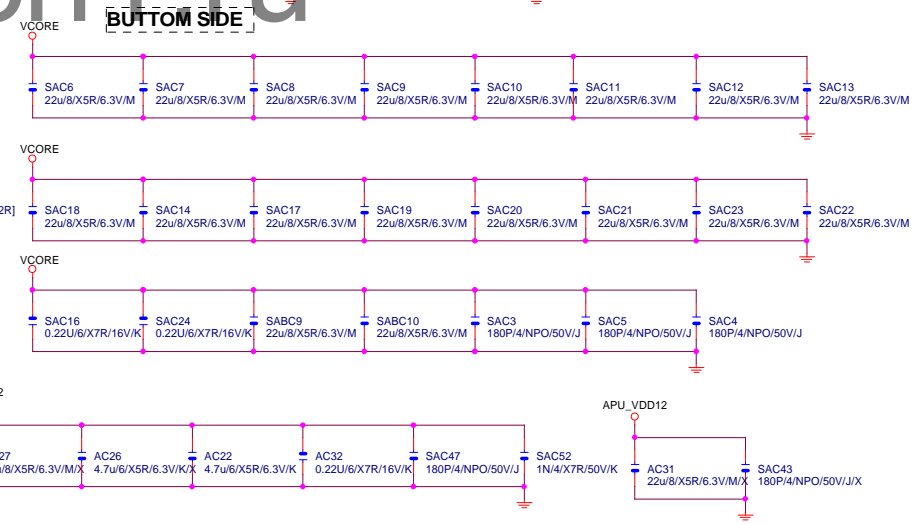
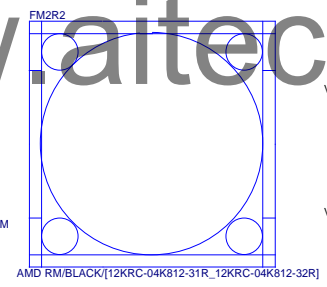


PCIE\_X16 Cross Moat CAP

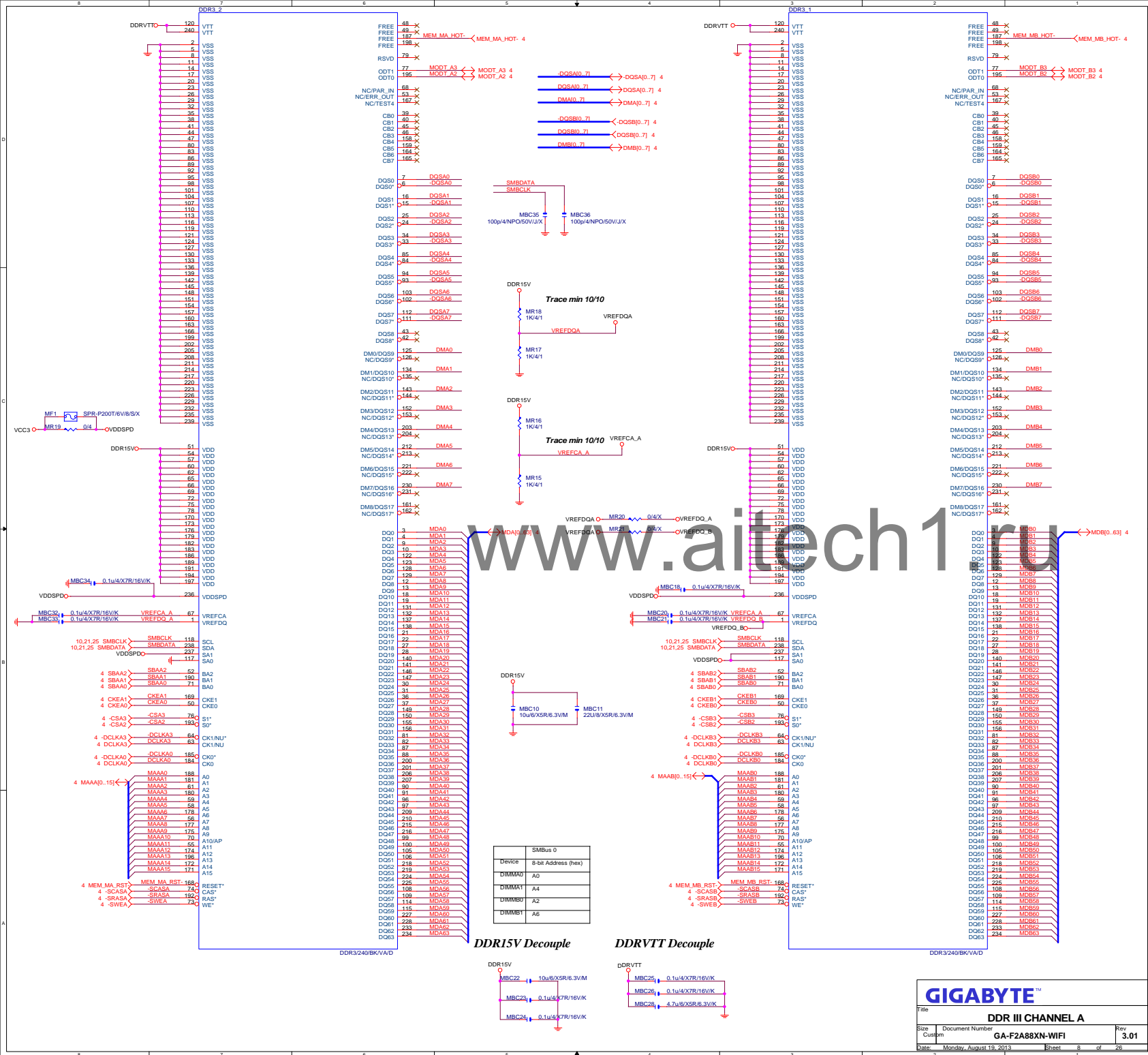
Place close N13, M14 pin inside  
the backplate cavity opening.



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GIGABYTE™			
Title APU POWER & GND			
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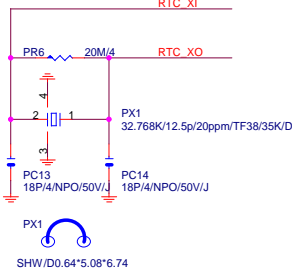


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

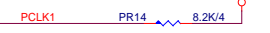
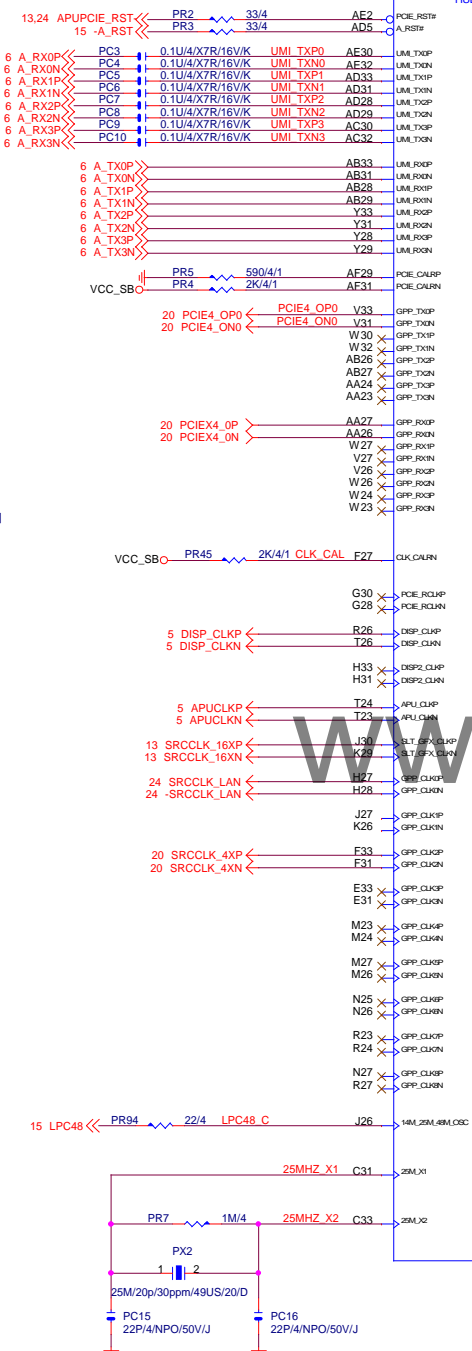
## S.B HEATSINK



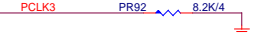
SB\_HS[12SP2-SA0301-01R\_12SP2-SA0301-02R\_12SP2-SA0301-03R]



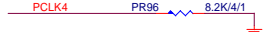
## For APU PCI\_E devices.



Low: Force PCIE GEN1, Up: Allow PCIE GEN2



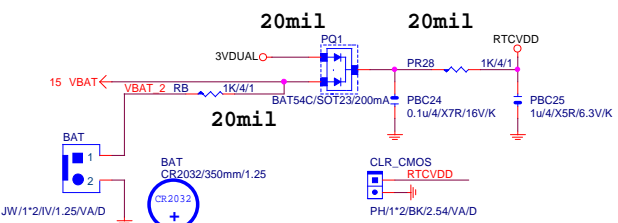
**PULL HIGH** USE DEBUG STRAPS  
**PULL LOW** IGNORE DEBUG STRAPS  
DEFAULT



CLKGEN Mode: Only for integrated clock mode.



**LPC\_CLK0** **LPC\_CLK1**  
**PULL HIGH** IMC ENABLED CLKGEN ENABLED  
**PULL LOW** IMC DISABLED CLKGEN DISABLED  
DEFAULT

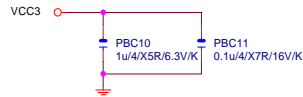


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

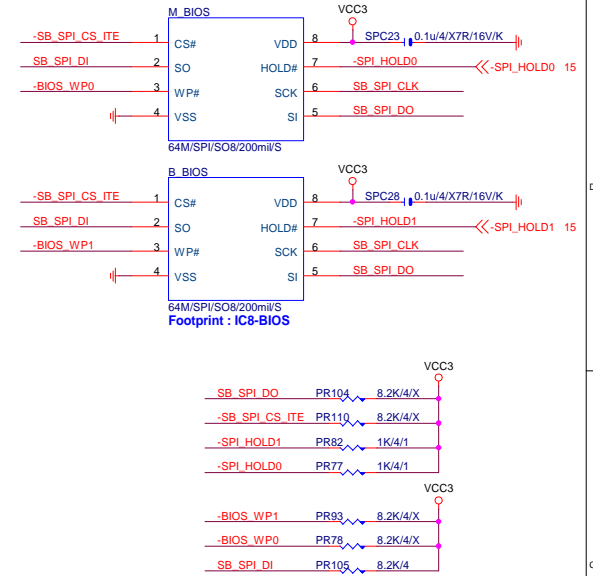
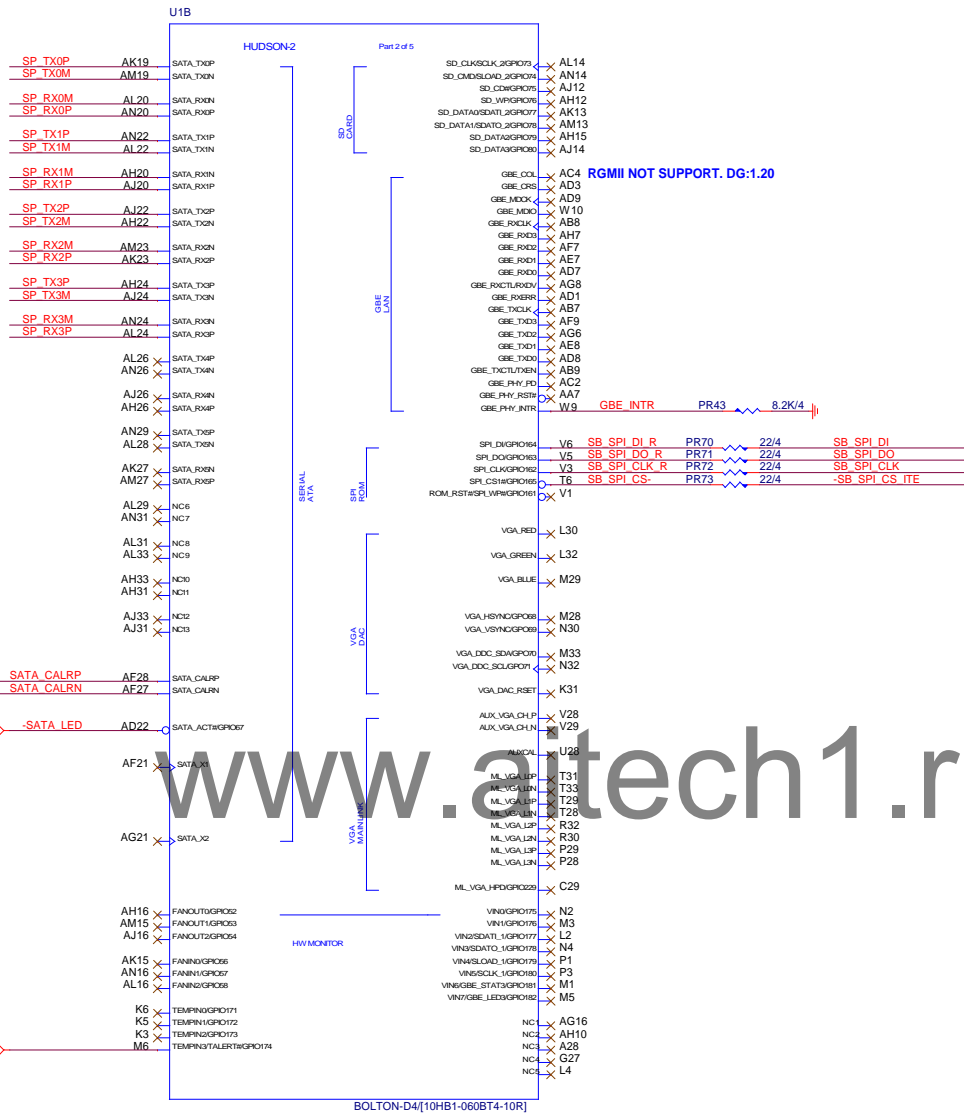
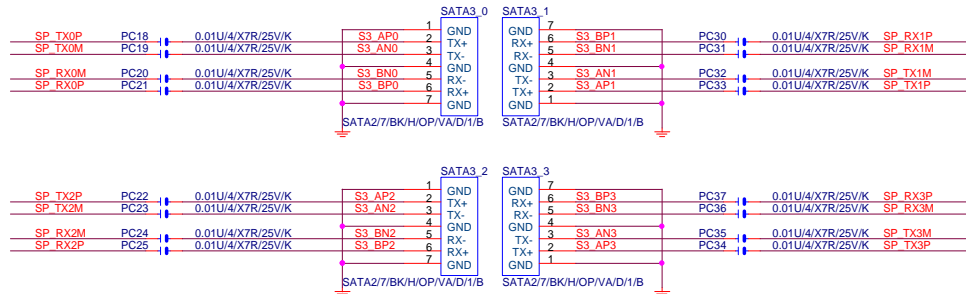
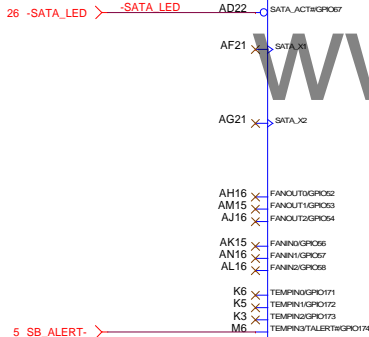
**GIGABYTE**  
Title: **Hudson D4 PCIE/PCI/CPU/LPC**  
Size: Custom  
Document Number: **GA-F2A88XN-WIFI**  
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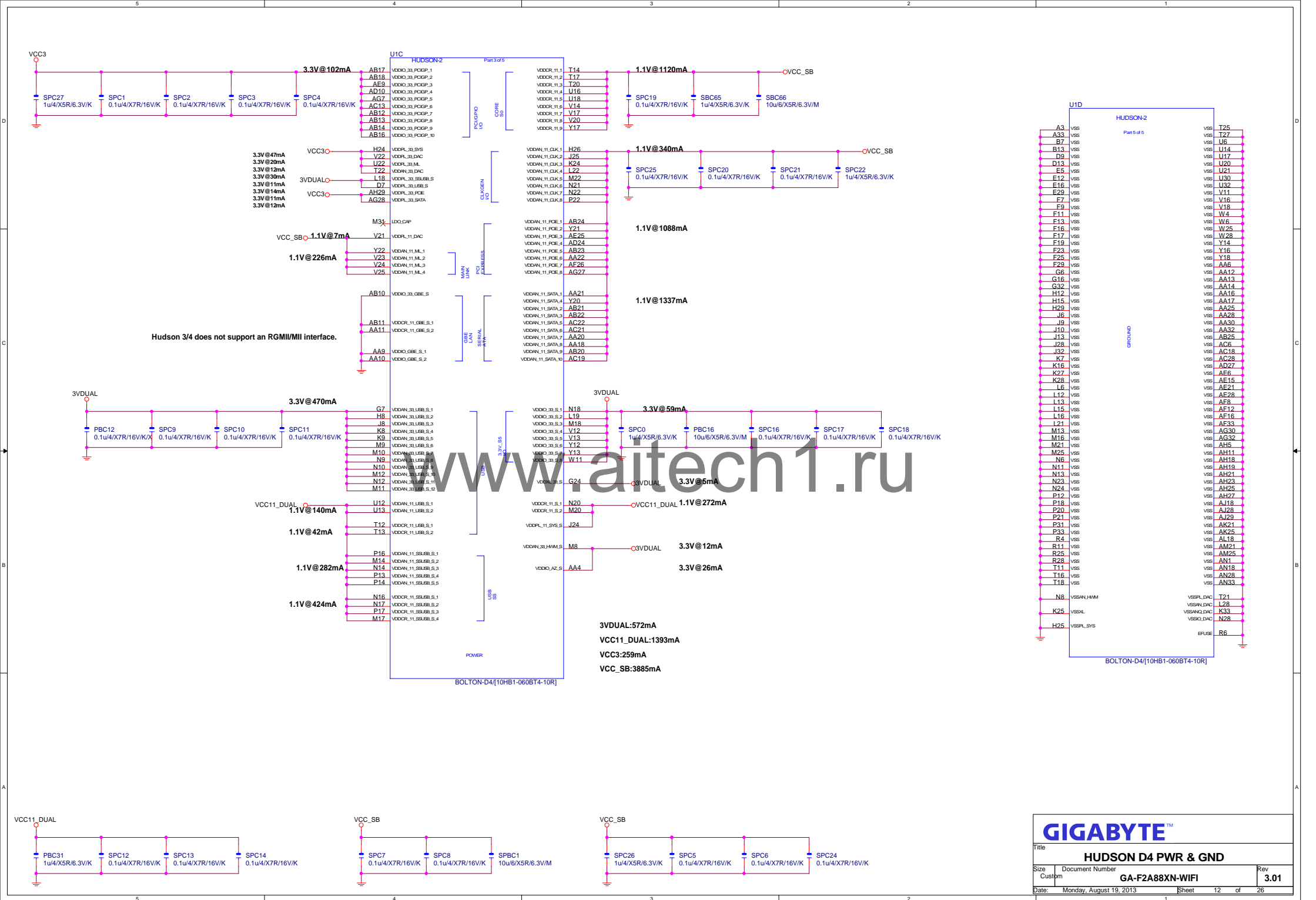


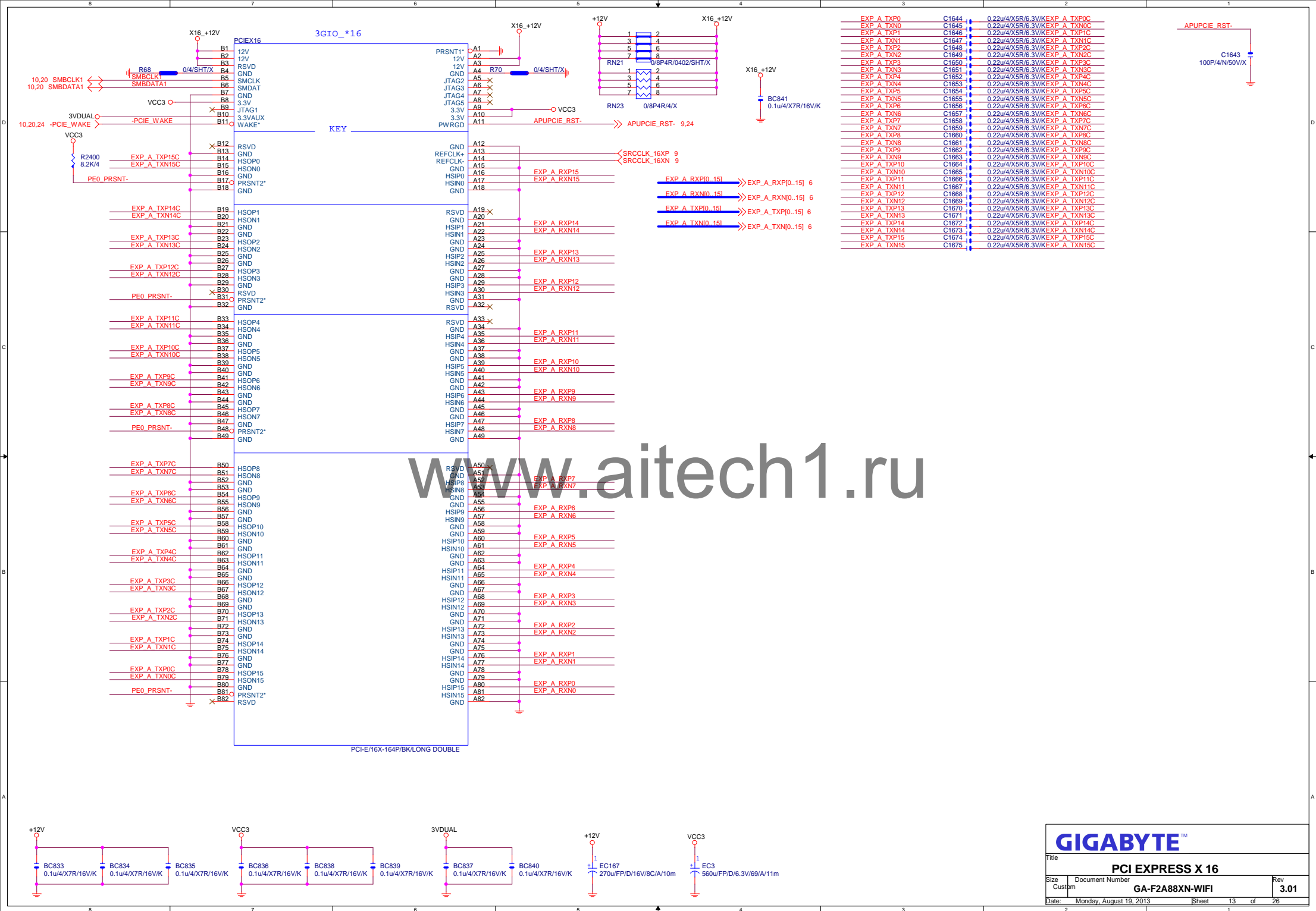


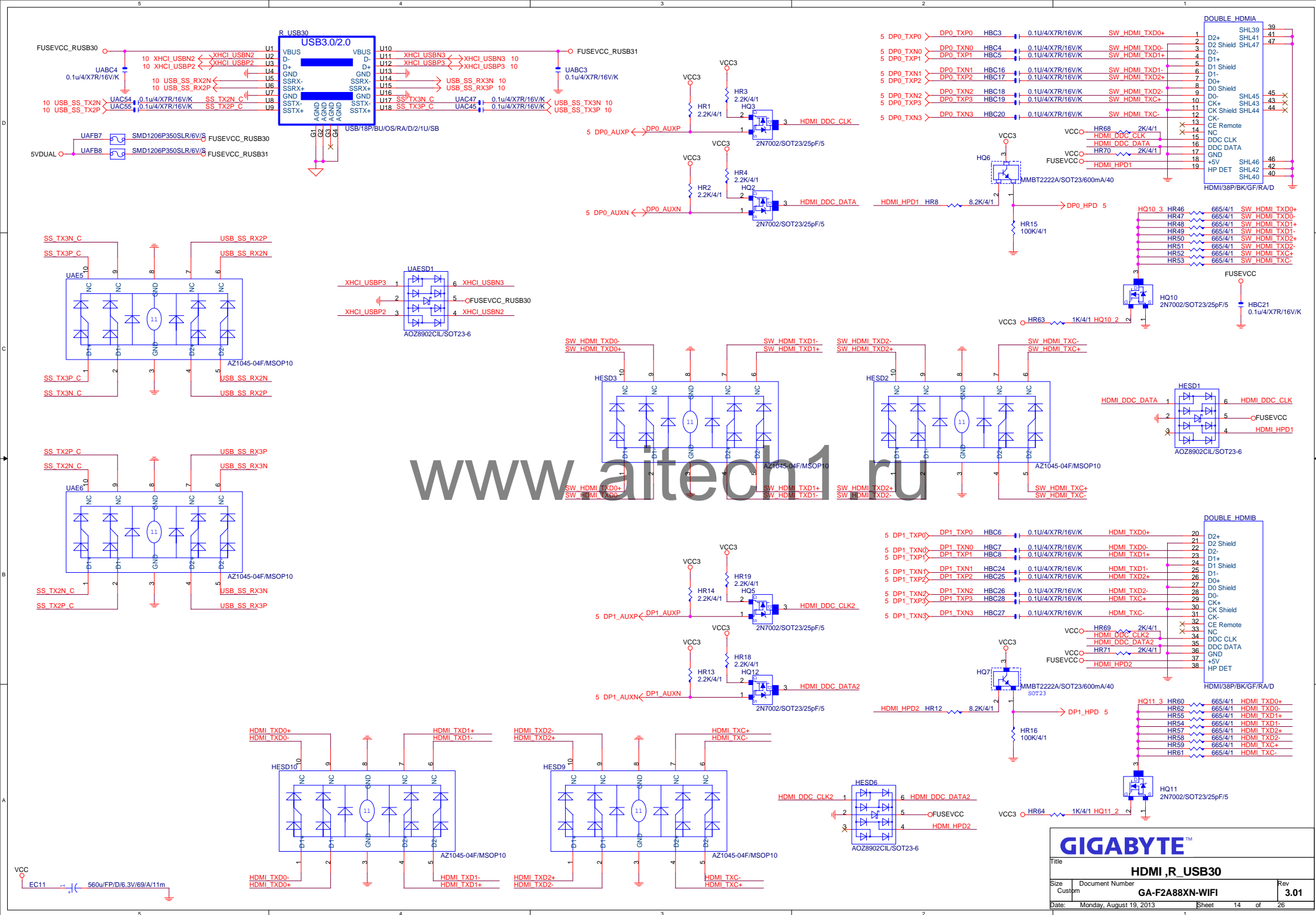
SATA 6~7 for Hudson D4.

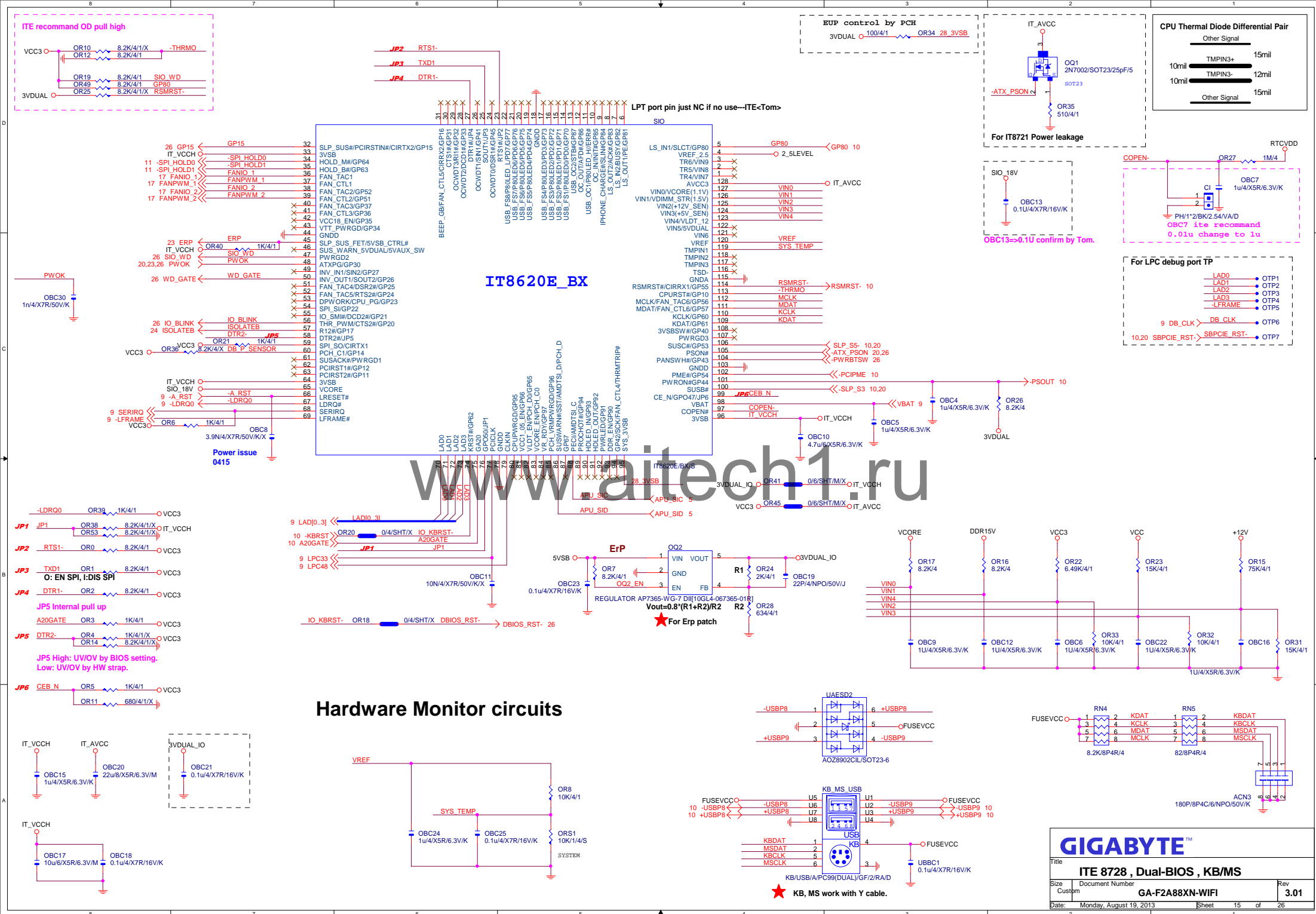
PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U1



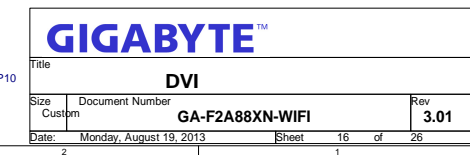
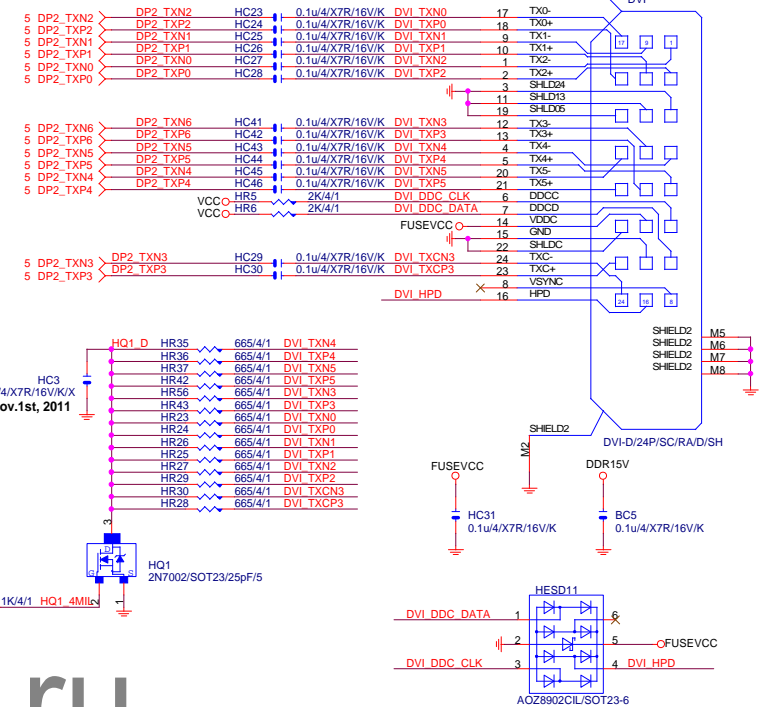




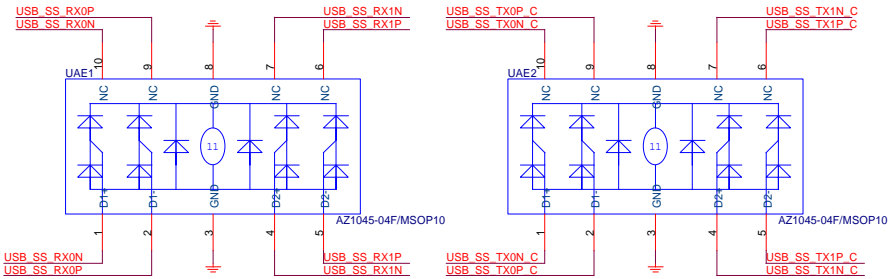
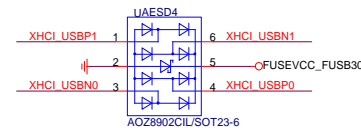
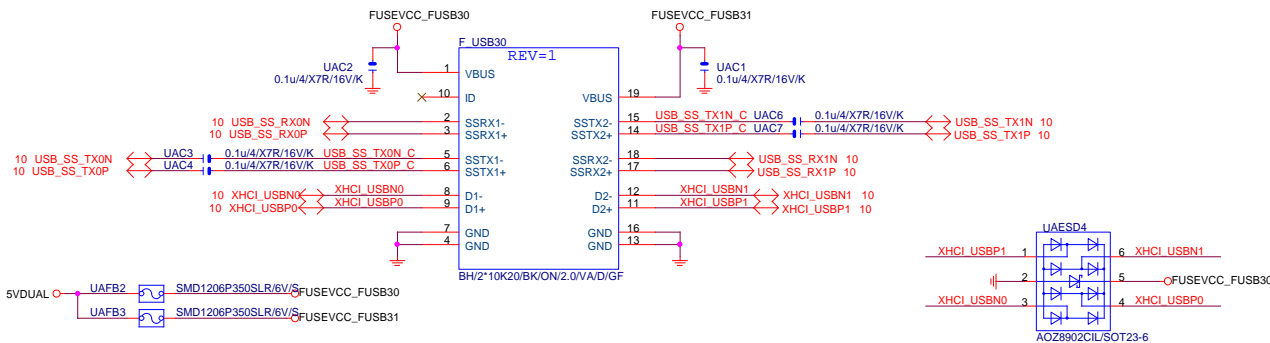






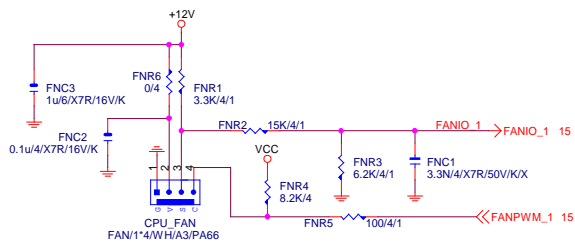




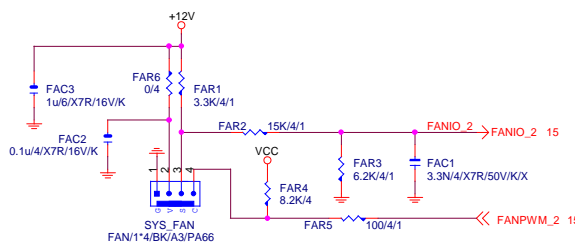


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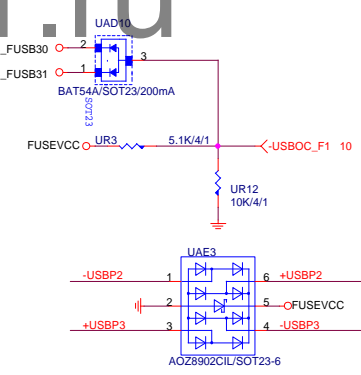
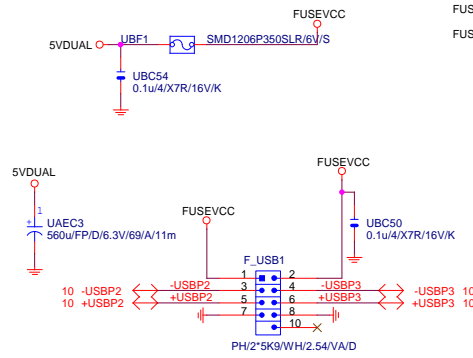
CPU SMART FAN



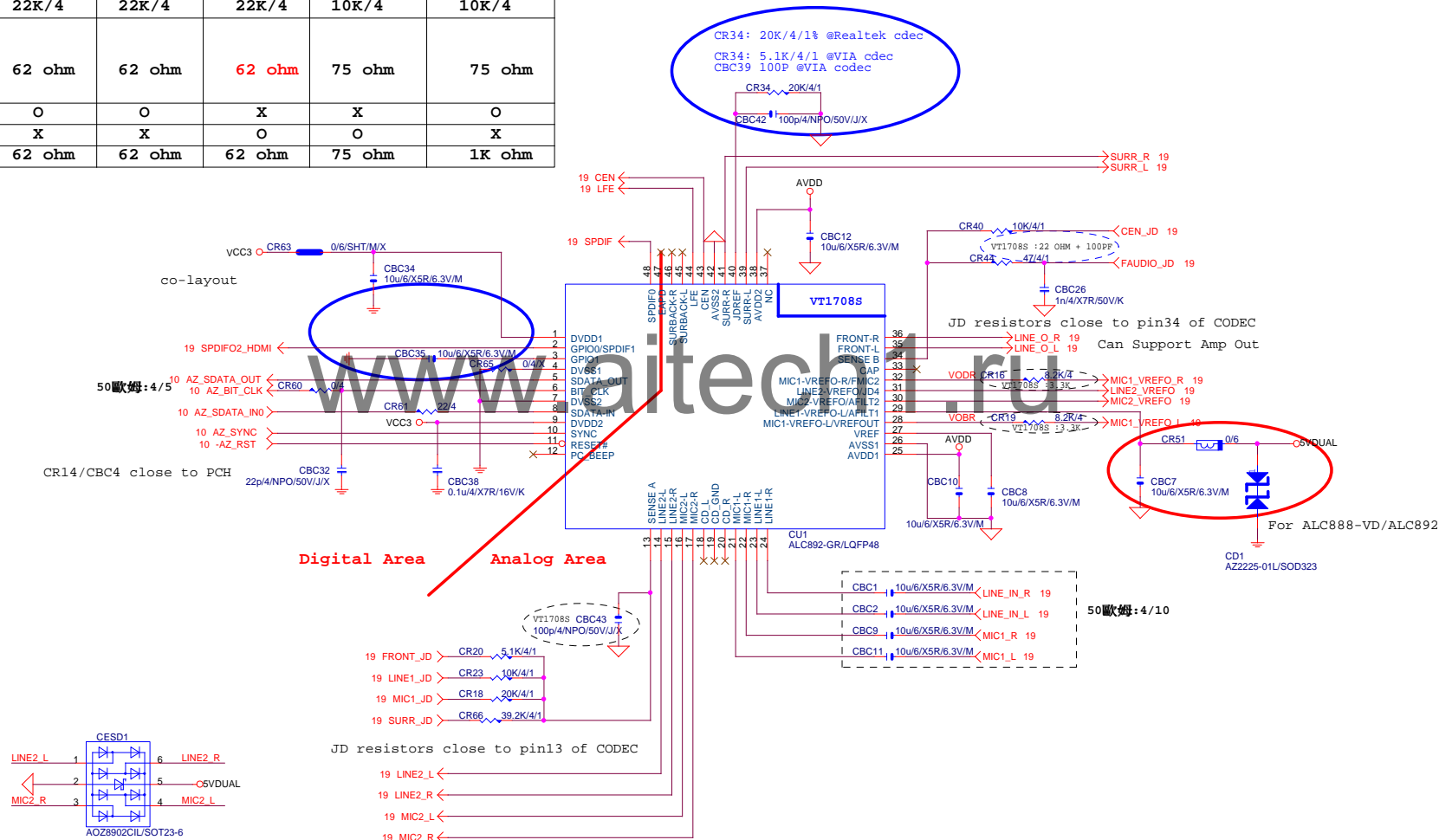
SYSTEM FAN1



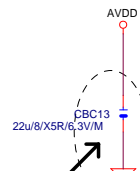
FRONT SIDE USB1



	ALC662	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	X	O	O	X
CR64	X	X	X	X	0.1u/4
CBC35	O	O	X	X	O
CR44/CBC6	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR31	X	O	O	O	O
CR30	O	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CR34	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CBC39/CBC40	N/A	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR11/CR4/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	O	X	X	O
CD2/CD3/CQ3/CQ5	X	X	O	O	X
CR1/CR14/CR17/CR22	62 ohm	62 ohm	62 ohm	75 ohm	1K ohm

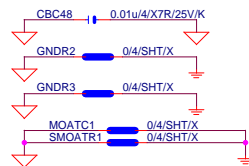


## CODEC POWER/EMI PAD

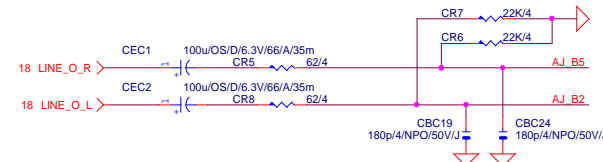


上ALC892時,此顆電容要保留

ADD CD2 For ESD PROTECT DIODE

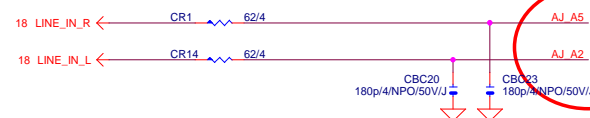


## LINE-OUT



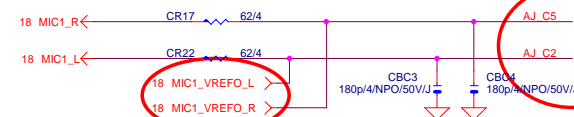
Only reserved For ALC888

## LINE-IN

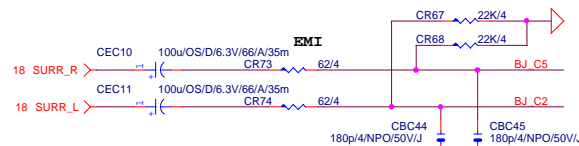
Verify MIC function  
in LINE-in

For 889A/888

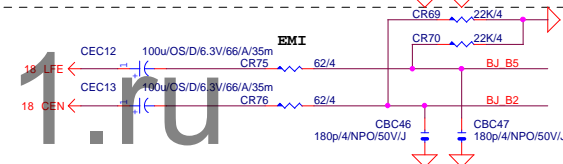
## MIC-IN



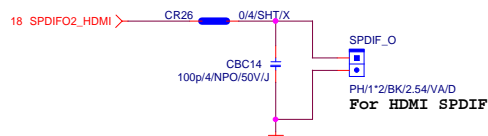
## SURROUND



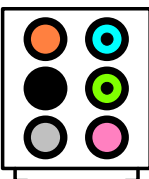
## CEN/LFE



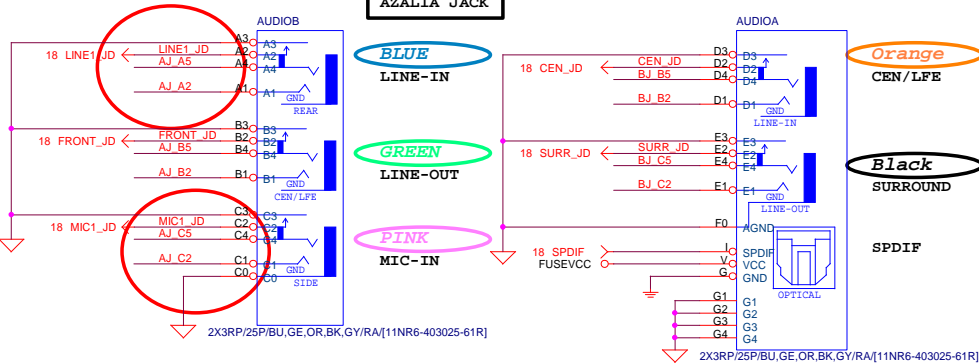
## SPDIF\_OUT



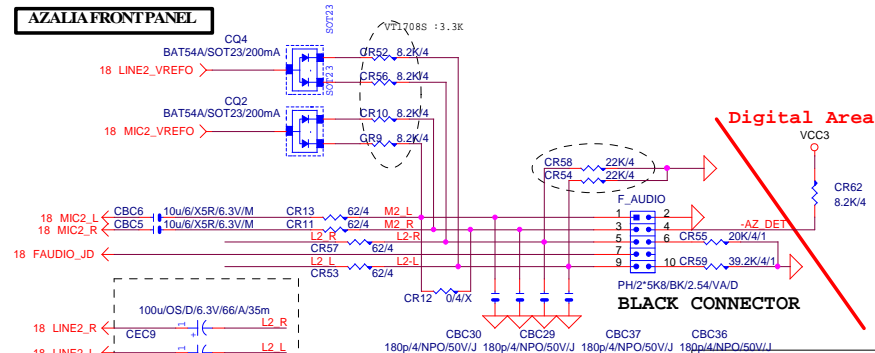
## AZALIA JACK



## AZALIA JACK

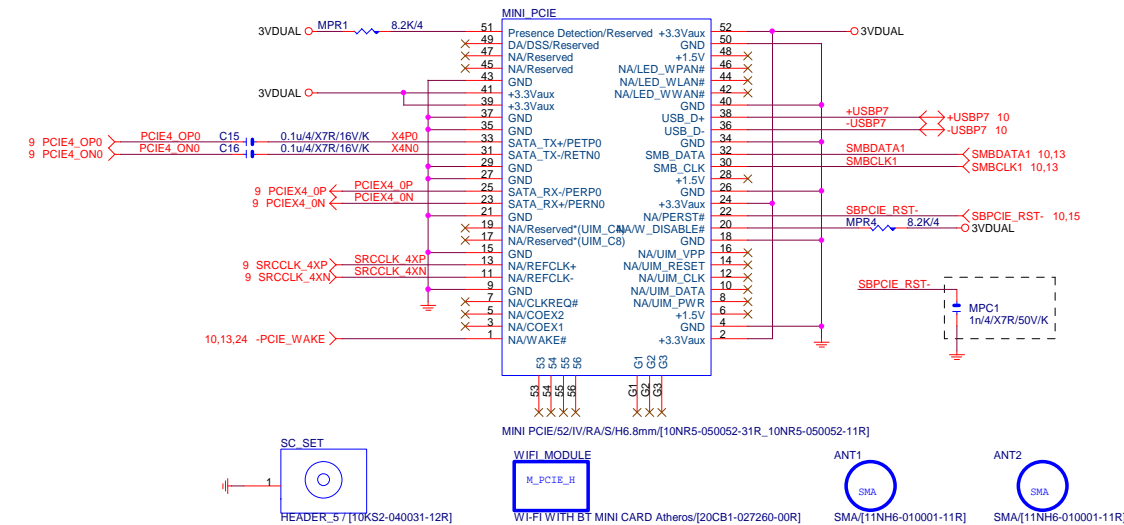
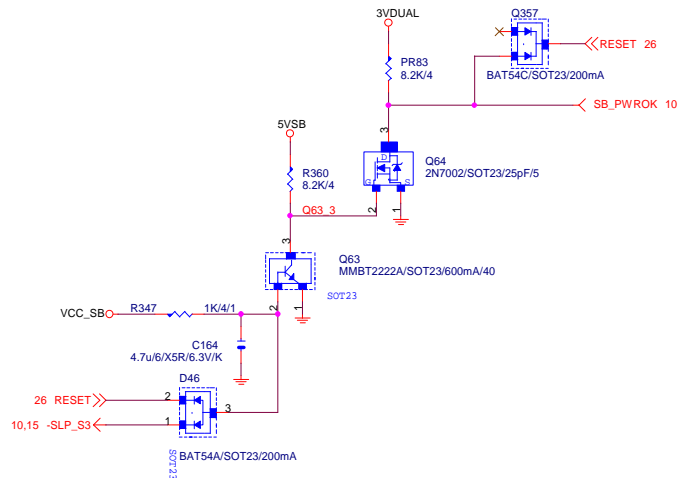
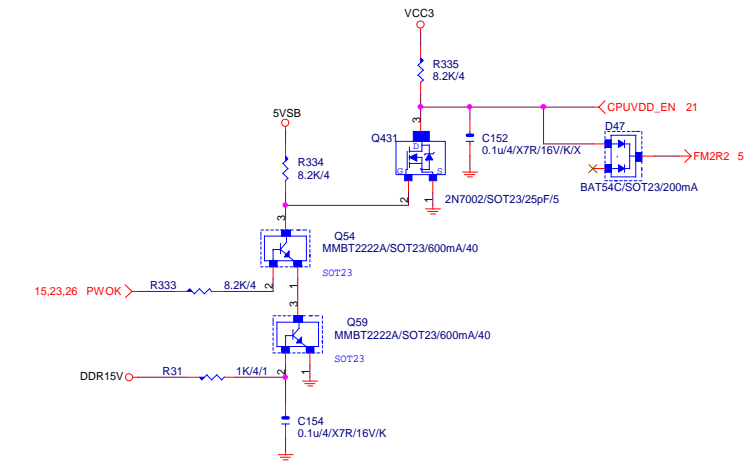
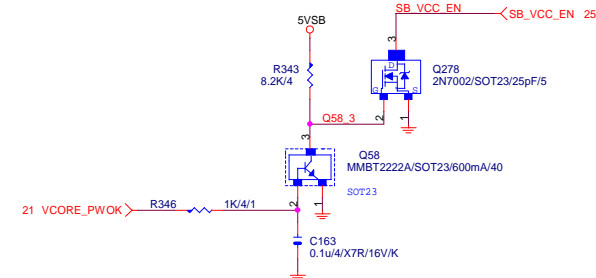
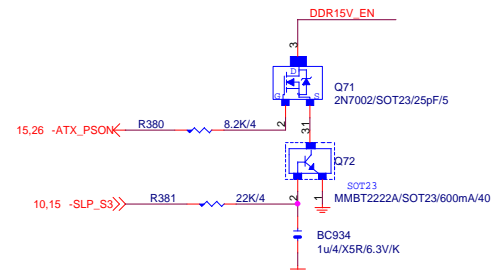
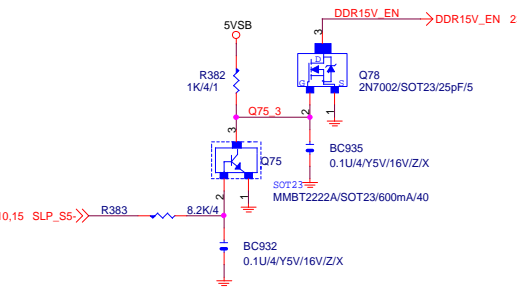


## AZALIA FRONT PANEL



GIGABYTE™

Title			
AUDIO JACK			
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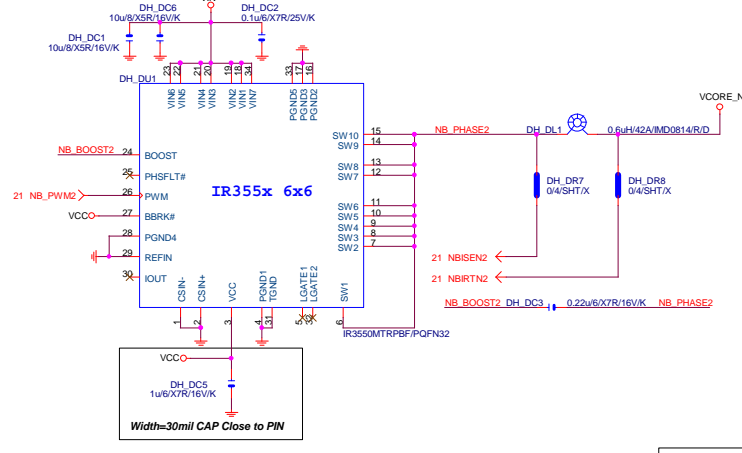
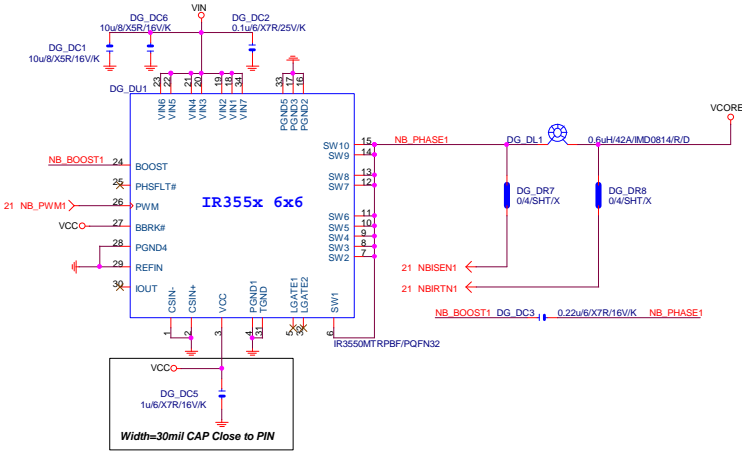
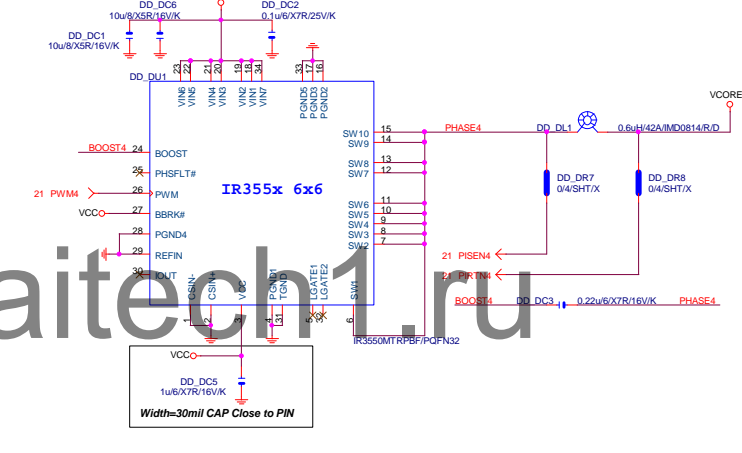
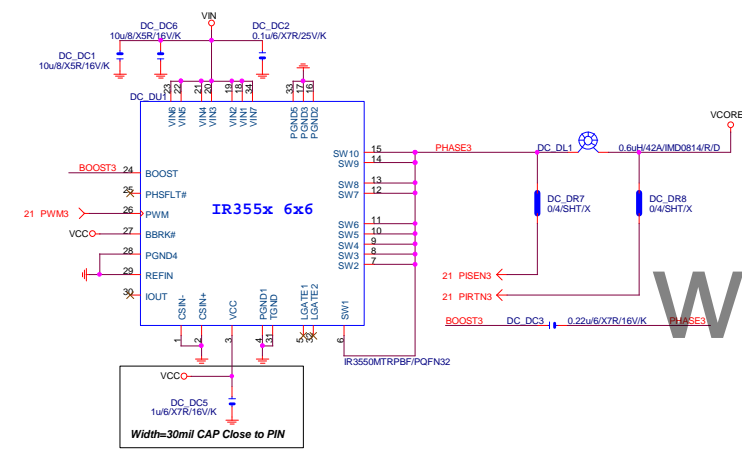
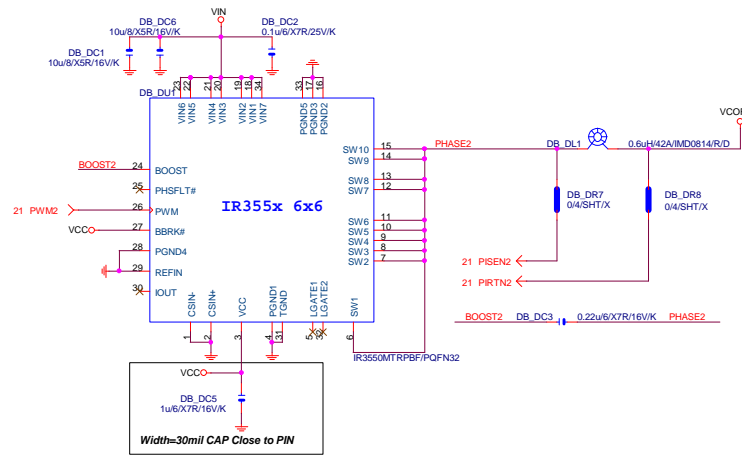
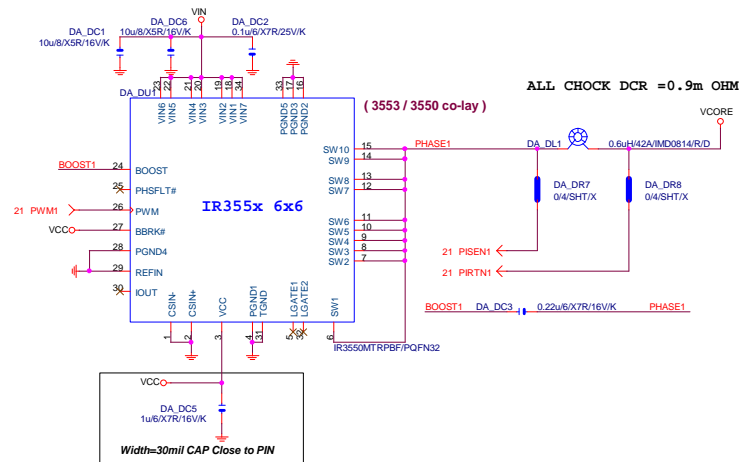


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GIGABYTE™			
Title POWER SEQUENCE ,MINI_PCIE			
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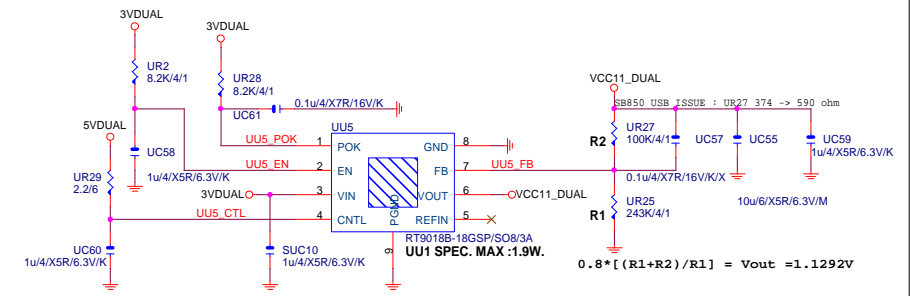
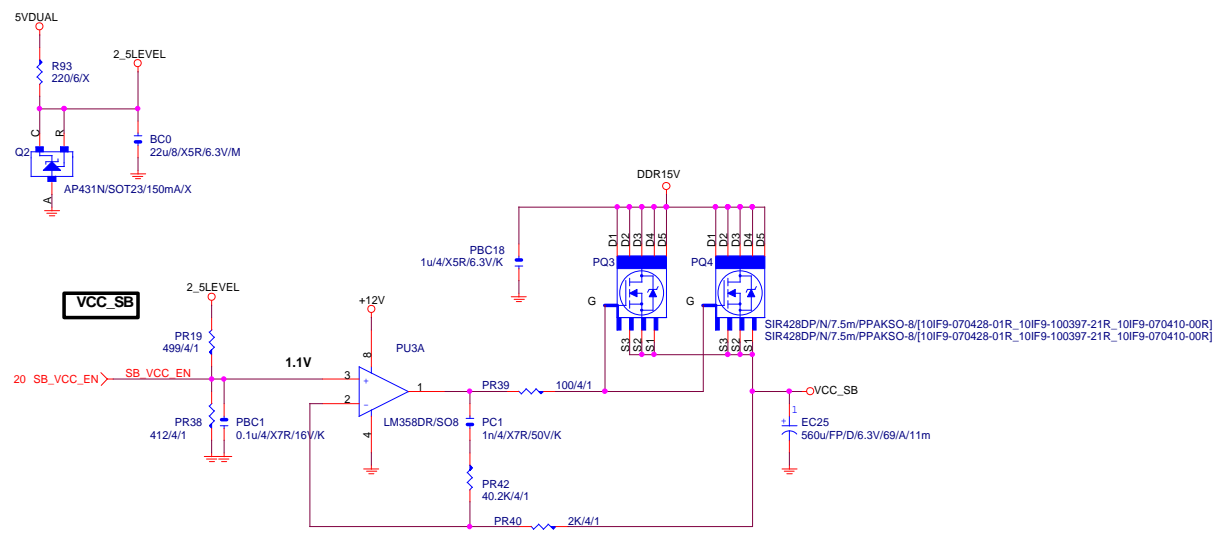




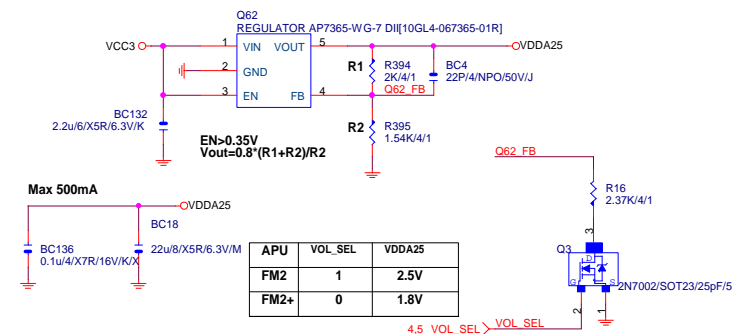
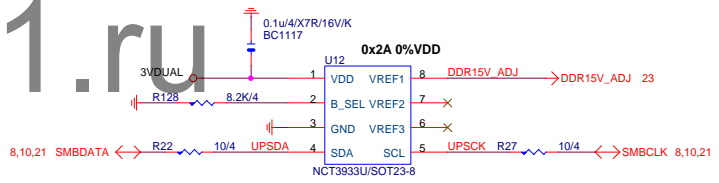
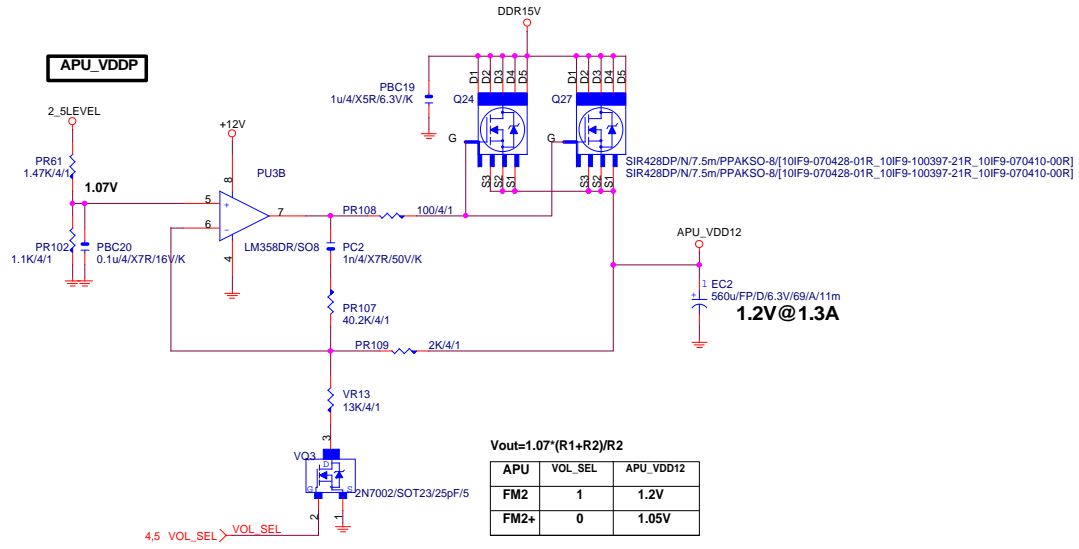








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$V_{out} = 1.07 \cdot (R1 + R2) / R2$

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

**GIGABYTE**™

Title: **VCC\_SB , APU VDDP, VCC11\_DUAL, VDDA25**

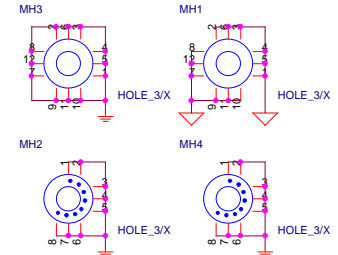
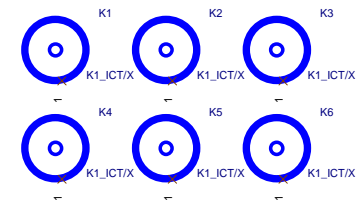
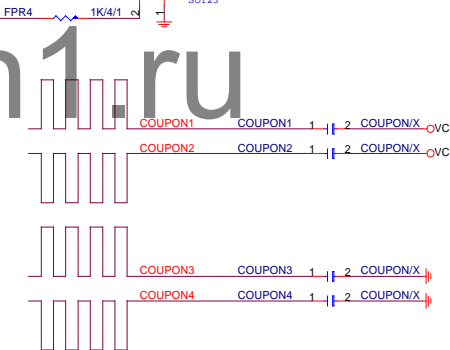
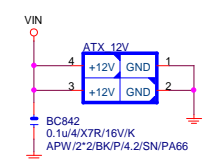
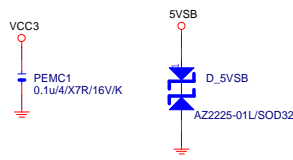
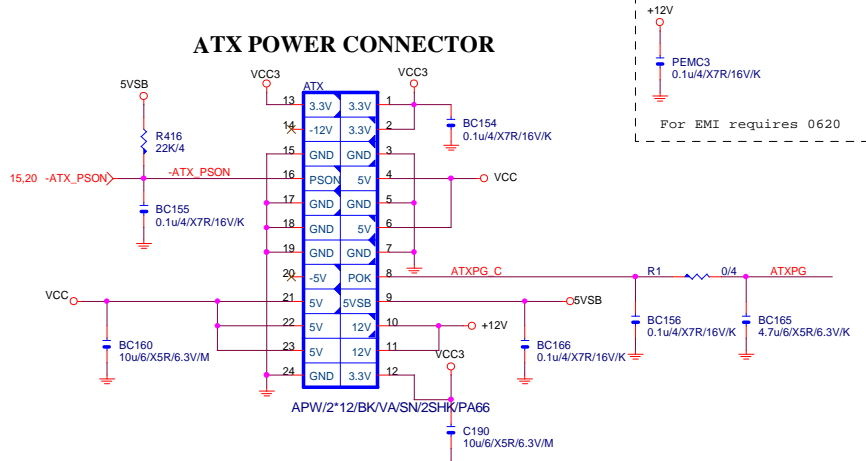
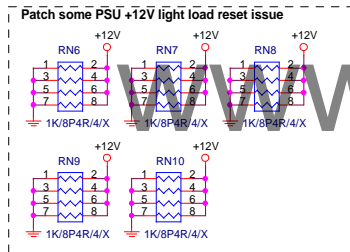
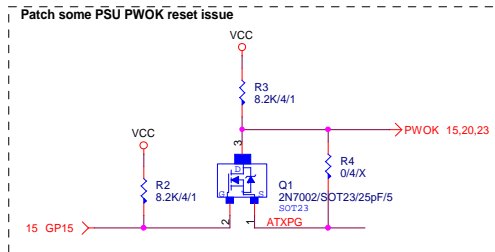
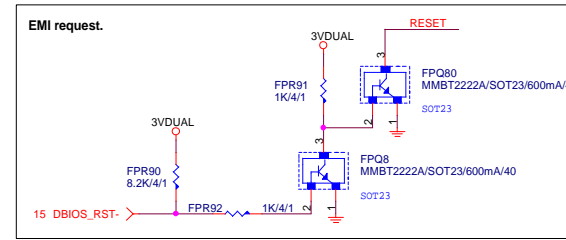
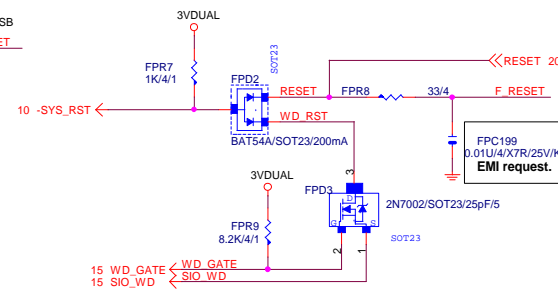
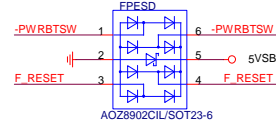
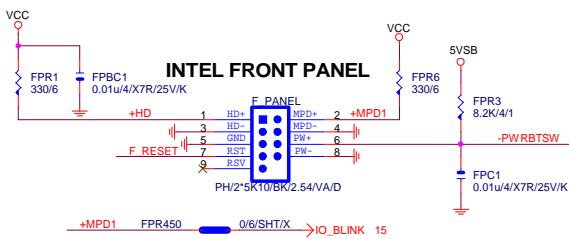
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Title: **ATX, FRONT PANEL**

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